Programming E1-CEPT modes of the 29C96

Introduction

The MHS's 29C96 is a complete T1-DS1/E1-CEPT framer. This framer is connected to one side on a PCM bus (from one at 6.176/8.192MHz to four PCM bus at primary rate) and on the other side to a line driver by a bipolar line at primary rate. The framer is in charge of formatting the PCM frame into different types of multiframe following the chosen mode by provinding synchronization and signalling pattern inside time slots 0 and 16. It is also in charge of extracting signalling and alarm bits from the line and providing reports to the processor. The framer has also time slots switching capabilities which allows the user to route 32 time slots coming from the PCM side to the 32 time slots located on the line side in any order. The 29C96 can manage the line driver by using a specific serial interface. This serial interface is common to all the MHS's 29C3xx line transceivers.

Main features

- Time Slots Switching.
  The time slot switching matrix located inside the 29C96 allows you to extract a maximum of 32 time slots from the PCM side and route these ones on the line outputs in any order. The transmit order is the same than the receive order i.e. the switching matrix is shared between the transmit and receive block. If a time slot is not validated, the received TS (on the PCM side) will be Hi-Z and the transmitted bipolar TS will be filled with a random byte or the byte contained into IDLE register if selected.
- Specific Serial Interface.
  This specific serial interface is used to read and write into the line driver. All the write and read cycles are generated by the 29C96. The read operation is only processed by the 29C96 when a high to low transition has been detected on the /INT300 pin. The write cycle is processed when the user writes into the 29C96 at @1EH.
- Framing mode.
  The synchronization pattern is forced into the TS0 on the transmit side and searched into TS0 on the receive side. Depending on the selected mode, some signalling pattern can be also introduced into TS16. If the synchro pattern has been recognized (according to G706 annexe B) the framer will be placed into multiframe mode and will be able to

Main registers and use

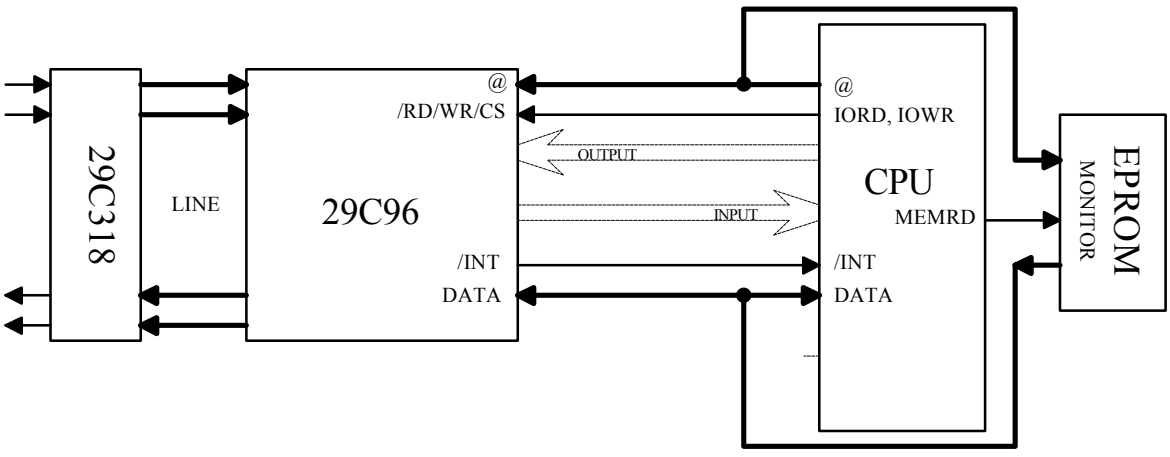
- Registers generating an interrupt :
  Only three registers generate an interrupt when a bit inside these ones changes from '0' to '1'. These three registers are ALARM (@00H), ERROR (@01H), MEMORY STATUS (@02H). The interrupt is cleared when the register causing the interrupt is read. We can consider these interrupts as 'one shot' i.e. a stable state doesn't generate an interrupt.
- Registers reporting an internal status :
  Two registers show the status of internal mecanisms. These two registers are SYNCHRONIZATION STATUS (@04H) and ALARM STATUS (@1FH). These two registers are used to provide complementaries information when a corresponding interrupt has been generated. For example, if the 29C96 receives a continuous RAI, one interrupt will be generated (ERROR.Ya set to '1') and then a polling on the ALARM STATUS register will indicate when RAI will disappear (ASR.RAIS set to '0').
- Registers used to start transmission/reception :
  The first register to write is the MODE register (@05H). With this register your choose your framing mode, your rate, your signalling mode. For CEPT, two framing modes are allowed and three signalling modes are avalaible.
  The second register to write is the PCM MODE register (@1AH). With this register the 29C96 can be set as "slave" (= FSC signal is provided to the 29C96) or as "free-running" (= FSC signal is provided by the 29C96) : see FRUN bit.

The PCM interface must be validated : see PCME bit. After that, the number of PCM bus (from 1 to 4) and the number of TS has to be defined : a E1 (PCM)-T1(line) connection can be realised.
The third action is to fill all the TSSR registers (from @60H to 7FH) and enable the corresponding channels. Depending on your line rate, you will enable 24 or 32 channels and 1 to 4 PCM bus.
The fourth register to write is the LINE CONTROL register (@07H) which allows the 29C96 to start frame alignment research if a toggle is applied on the REFRAME bit.
The fifth register to write is the FRAMER CONTROL register (@08H) which allows to start transmission on the PCM line by setting to one the STRANS bit.

- Extra features
  - Transmit control register (TCR)
    This register provides extra-features during transmission like sending AIS...
  - Mask registers (MASK)
    These registers enable or not the mask on the corresponding interrupt. If these registers are filled with FFH, no interrupt will be masked.
  - Transmit/receive signalling (T/RSR)
    The signalling data come from two sources : the fisrt one is the internal source - the transmit signalling RAM (TSR registers) has to be filled before starting transmission - the second one is the external source via XABCD pin. Depending on the chosen mode, the signalling data extracted from the frame will be placed into the internal receive signalling RAM (RSR registers) or routed to the RABCD output pin.
  - Transmit/receive spare bit register (T/RSBR)
    This register is used when a non automatic mode is selected (E bit will be taken into this register or placed into after extraction) or when the user wants to drive/extract the Sn bits (avalaible in automatic mode also).
  - Idle registers (IDLE)
    These registers are used on the transmission side to overwritre up to 32 channels with a byte designated by the user.
  - Receive mask register (MCR)
    These registers are used on the receive side to overwrite up to 32 channels with a byte selected by the user.

Example of program :

Schematic



In this example, the 29C96 is IO mapped from 1000H and the 29C318 is connected to the 29C96.
The monitor located into the EPROM provides a simple user interface and simple commands like :

O means Write ('Output port'<@>,<data>). Two parameters : destination address and data provided by CPU.

I means Read ('Input port'<@>). One parameter : destination address provided by CPU. The returned content is written under the command.

A comment is always preceded by "*"
The 29C96 is programmed in E1/CRC4/transparent mode with automatic mode for E bits generation. The HDB3 coder/decoder is also used.

```
* ------ reset
O 1008,01
*-------- Free-running mode
O 101A,08
* ------ MODE : CEPT/CRC4
O 1005,03
* ----- LCR : HDB3
O 1007,80
* ----- RMR : no receive channels masked
O 1013,00
* ----- TCR : no alarm generated
O 1004,00
* ----- MCR0,1,2,3 : no mask channel
O 1014,00
O 1015,00
O 1016,00
O 1017,00
* ----- FCR : ACSI (automatic mode set) -> no use of T/RSBR
O 1008,08
* ----- IDLE : no idle byte
O 100E,00
* ----- ICR0,1,2,3 : no idle channels
O 100F,00
O 1010,00
O 1011,00
O 1012,00
* ----- TSSR : TS0 from PCM0 is routed on TS0 of the line, TS1 on TS1...
O 1060,80
O 1061,81
O 1062,82
O 1063,83
O 1064,84
O 1065,85
O 1066,86
O 1067,87
O 1068,88
O 1069,89
O 106A,8A
O 106B,8B
O 106C,8C
O 106D,8D
O 106E,8E
O 106F,8F
O 1070,90
O 1071,91
O 1072,92
O 1073,93
O 1074,94
O 1075,95
O 1076,96
O 1077,97
O 1078,98
O 1079,99
O 107A,9A
O 107B,9B
O 107C,9C
O 107D,9D
```

```
O 107E,9E
O 107F,9F
* ----- PMR PCM enable and free-running confirmed
O 101A,2B
* ----- MASK0,1,2 : no mask on interrupt
O 1009,FF
O 100A,FF
O 100B,FF
* ---- no local loopback, no loopback PCM
O 1006,00
* -----  LOOPBACK inside 318
O 101E,40
* ---- no  RSR signaling
* ---- no TSR signaling
* ---- LCR : HDB3 29C96 +ALFA+toggle reframe
O 1007,85
O 1007,84
* ---- FCR : autom mode + start trans
O 1008,88
O 1008,98
* transmission started : wait for interrupts
```

In order to know if the 29C96 has succeded in synchronization operation, we have to look at the Synchronization Status Register. The three bits (SYNC, BFA, MFA) have to be set by the 29C96 to one to indicate that a multiframe alignment has been found according to G.706 Annexe B. When BFA or MFA bits change from '0' to '1', this change is reported into FAach bit (see ERROR register). Each time FAach change from '0' to '1', an interrupt is generated to the host processor. If the received frame contains frame but no multiframe alignment, only SYNC and BFA will be set to '1'. If none of these bits are set to one, it indicates that no frame alignment research has been done (due to no toggle on REFRAME bit for example) or no alignment pattern has been found corresponding to the chosen mode.

According to G.706 annexe B, if within the 400ms timer, the multiframe alignment has not been found twice within 8ms period, the 29C96 jumps into double frame mode (MFA is set to '0' and FTEMPO, LFA, CRC4 are set to '1'). To automatically restart a complete multiframe alignment research after FTEMPO event, ALFA and ALMA has to be set to one during initialization. According to ETSI specifications (EST300:011), no RAI will be sent 500 ms after FTEMPO event. The CRC4 bit signals that the component has jumped from multiframe to double frame mode.

Upon reception of 3 contiguous /FAS or bit 2 errors, LFA is set to '1' and an alignment research will automatically restart if ALFA has been set to '1' during initialization. Upon reception of 915 over 1000 CRC4 multiframe patterns received with error status, LMA (Loss of Multiframe Alignment) occurs. LMA brings LFA. When LFA has been set to '1' by the 29C96, the alignment research mecanism is totaly resetted. If ALFA has been set to one during initialization, a frame alignment research will be automatically started by the 29C96 after LMA event.

An automatic mode for E bits sending is also avalaible. This mode is validated by setting ACSI to '1'. The automatic mode is used to automatically generate E bits at the good polarity during multiframe alignment research and then set E bits to "0" in the transmitted frame each time a CRC error is detected in the incomming frame (within 1s according to G.706). The number of E bits set to "0" is equal to the number of detected CRC errors and in the case of contiguous CRC errors into the received frame, the transmitted E bits set to zero are also contiguous.

An automatic mode for RAI is also avalaible. This mode is validated by AYa set to '1'. When AYa is set to '1', a RAI will be automatically generated by the 29C96 to the remote side when an LFA event occurs. This RAI is sent until a BFA state is reached. It is not possible to force a RAI sending with Ya bit set to '1' when AYa is set to '1'.

A way to control the start of transmission is to observe signals on XFCLOCK and XMFCLOCK pins. If the transmission mecanism is correctly initialized and validated, XFCLOCK will provide a 8Khz frequency signal and XMFCLOCK will provide a 150µs or 2ms frequency signal. If none of these signals are presents, it indicates that the transmission mecanism has not been properly validated or some required clocks to correctly transmit are not provided.

Example of program (continued):
(X = don't care)

I1000
XX
I1001
8X
I1002
XX
I1003
C3

The microprocesssor has to perform at least four reads each time an interrupt is generated. At the beginning, the first interrupt is generated when the internal synchronization mecanism jumps into BFA state (bit FAach set to one). The E bits are continuously extracted from the receive side (as soon as the first multiframe alignment is detected) i.e. if the extracted E bits are continously received at '0' during the alignment research, this state will not generate an interrupt. But this state can be detected by reading EBIT0 and EBIT1 bits located into SSR.

I1000
XX
I1001
8X
I1002
XX
I1003
C7

The second interrupt is generated when the internal synchronization mecanism jumps into MFA state (FAach bit set to one). At this moment the RAI detection mecanism will be enabled. Contrary to E bit extraction mecanism, if the 29C96 gains alignment on a multiframe carrying a continous RAI, this RAI will be detected. The receive mecanism reports also its internal state through RFCLOCK and RMFCLOCK pins. If the receive block is synchronized, RFCLOCK will provide a 8KHz frequency signal and RMFCLOCK will provide a 250µs or 2ms frequency signal.

Note on Transparent mode : The transmit block is totaly transparent if this mode is programmed. The receive block will be transparent when a pattern alignment will be recognized and BFA will be set to 1. This difficulty can be bypassed by using IMAx bits (PMR register) to route the data received on the bipolar line (RINN, RINP) to the AMIE output pin. By this way, the synchro block located into the receive block is shunted. An external multiplexer is then needed to route the data coming out from AMIE to the ROUTx PCM line.

After Synchronization step

When the 29C96 generates an interrupt, the host processor will read the first four registers located into the 29C96. Following the events reported into these four registers, the host processor will find a complementary information into SSR and ASR registers.
It is possible to disable the CRC4 check only on the receive side and continue to transmit multiframes with correct CRC4 into (see FCR./ENACRCH). It is also possible to totally disable the CRC4 function on receive and transmit side (see LCR.INHICRC4). In this case the transmitted CRC4 bits will be forced to '1'.
The NCHA bit located into PMR is only used in E1 mode. This bit allows E1 (on PCM side) -T1 (on line side) connection when in E1 mode this bit is set to '1'.
A management of Sn bits can also be performed even in transparent mode : MSR.RSBR and MSR.TSBR bits are set to one and generate an interrupt each time the RSBR is full or TSBR is empty.

If Multiframe alignment is not found

In case of multiframe initialization, if after 400ms the multiframe alignment is not found twice within 8ms, the 29C96 jumps into double-frame mode and ALARM.FTEMPO and SSR.CRC4 are set to '1'. The FTEMPO bit will signal that the timer has reached 400ms. The CRC4 bit will signal that all the CRC4 features has been disabled. RSBR and TSBR registers will be used to received and transmit Si/Sn bits.

Additional Information

For Additional information, please refer to the 29C96 datasheet.